

# DATA SHEET

## **74ALVCH162827**

20-bit buffer/line driver, non-inverting,  
with 30 $\Omega$  termination resistors (3-State)

Product specification

1998 Sep 29

IC24 Data Handbook

## 20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

# 74ALVCH162827

### FEATURES

- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive  $\pm 12$  mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and GND pins for minimum noise and ground bounce
- Integrated 30 Ω termination resistors

### DESCRIPTION

The 74ALVCH162827 high-performance CMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ALVCH162827 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NAND Output Enables ( $n\overline{OE}1$ ,  $n\overline{OE}2$ ) for maximum control flexibility.

The 74ALVCH162827 is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

To ensure the high impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

### QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f = 2.5\text{ns}$

| SYMBOL            | PARAMETER                               | CONDITIONS   | TYPICAL         | UNIT |    |
|-------------------|---|--|-----------------|------|----|
| $t_{PHL}/t_{PLH}$ | Propagation delay<br>nAn to nYn         | $V_{CC} = 2.5\text{V}$ , $C_L = 30\text{pF}$<br>$V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$ | 2.9<br>2.9      | ns   |    |
| $C_I$             | Input capacitance                       |  | 5               | pF   |    |
| $C_{PD}$          | Power dissipation capacitance per latch | $V_I = \text{GND to } V_{CC}^1$  | Output enabled  | 14   | pF |
|                   |   |  | Output disabled | 3    |    |

#### NOTES:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### ORDERING INFORMATION

| PACKAGES                     | TEMPERATURE RANGE                             | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|------------------------------|---|-----------------------|---------------|------------|
| 56-Pin Plastic TSSOP Type II | $-40^{\circ}\text{C to } +85^{\circ}\text{C}$ | 74ALVCH162827DGG      | ACH162827DGG  | SOT364-1   |

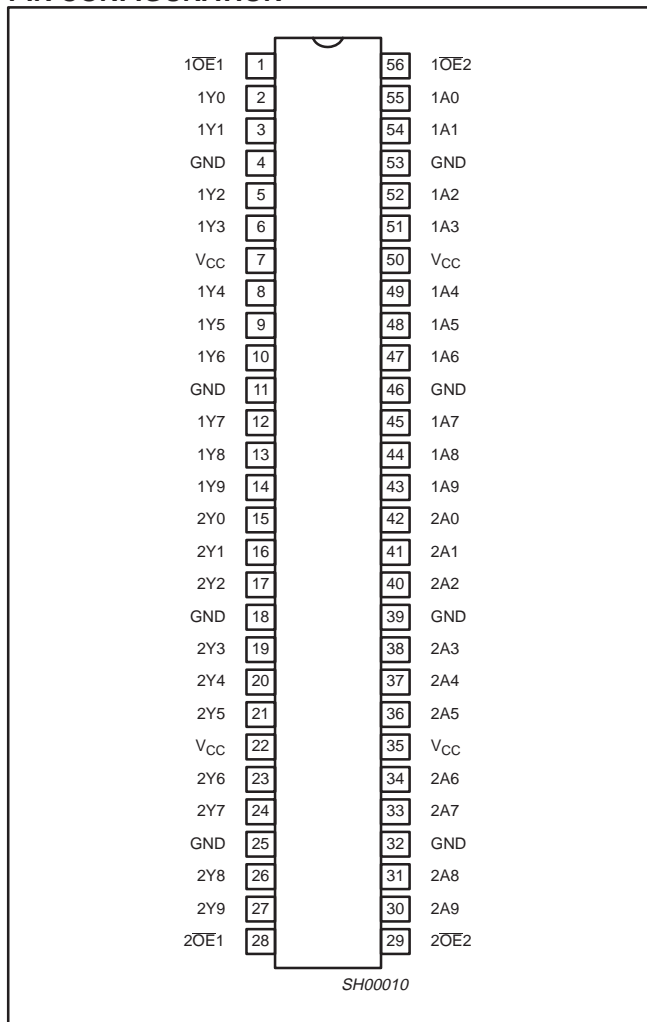
### PIN DESCRIPTION

| PIN NUMBER  | SYMBOL   | FUNCTION                          |
|---|--|-----------------------------------|
| 55, 54, 52, 51, 49, 48, 47, 45, 44, 43,<br>42, 41, 40, 38, 37, 36, 34, 33, 31, 30 | 1A0 - 1A9<br>2A0 - 2A9   | Data inputs                       |
| 2, 3, 5, 6, 8, 9, 10, 12, 13, 14,<br>15, 16, 17, 19, 20, 21, 23, 24, 26, 27       | 1Y0 - 1Y9<br>2Y0 - 2Y9   | Data outputs                      |
| 1, 56,<br>28, 29  | $1\overline{OE}1$ $1\overline{OE}2$ ,<br>$2\overline{OE}1$ , $2\overline{OE}2$ | Output enable inputs (active-LOW) |
| 4, 11, 18, 25, 32, 39, 46, 53   | GND  | Ground (0V)                       |
| 7, 22, 35, 50   | $V_{CC}$   | Positive supply voltage           |

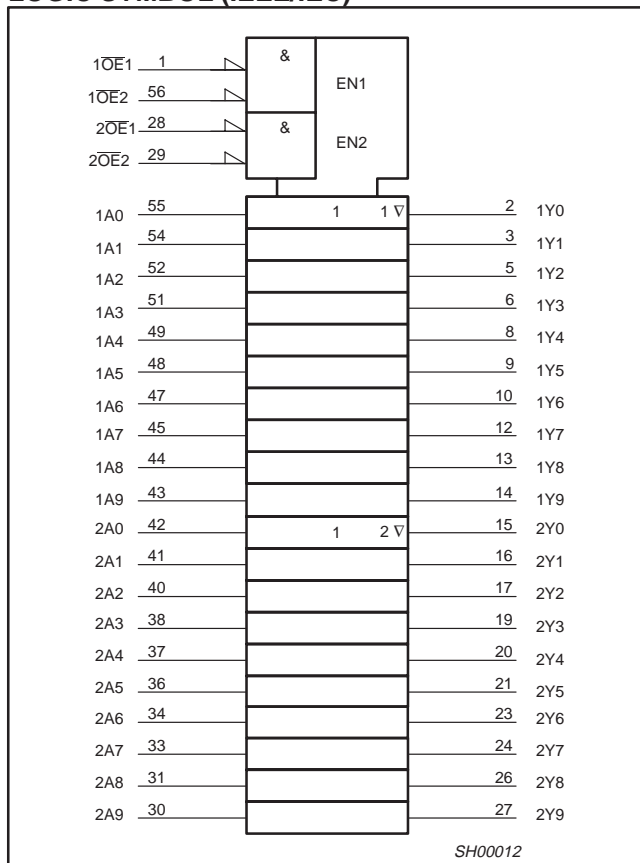
# 20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

74ALVCH162827

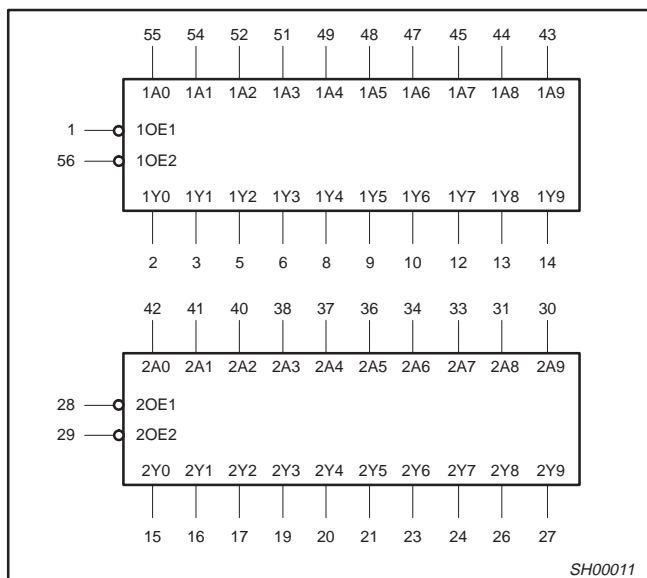
## PIN CONFIGURATION



## LOGIC SYMBOL (IEEE/IEC)



## LOGIC SYMBOL



## FUNCTION TABLE

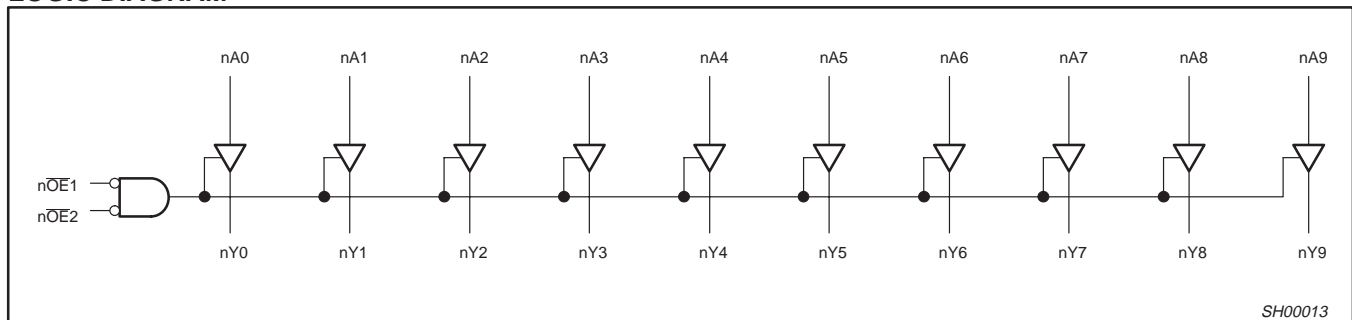
| INPUTS |      |     | OUTPUT | OPERATING MODE |
|--------|------|-----|--------|----------------|
| nOE1   | nOE2 | nAn | nYn    |                |
| L      | L    | L   | L      | Transparent    |
| L      | L    | H   | H      | Transparent    |
| H      | X    | X   | Z      | High impedance |
| X      | H    | X   | Z      | High impedance |

- X = Don't care
- Z = High impedance "off" state
- H = High voltage level
- L = Low voltage level

# 20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

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## LOGIC DIAGRAM



## RECOMMENDED OPERATING CONDITIONS

| SYMBOL                          | PARAMETER   | CONDITIONS                    | MIN | MAX             | UNIT |
|---------------------------------|---|-------------------------------|-----|-----------------|------|
| V <sub>CC</sub>                 | DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load) |                               | 2.3 | 2.7             | V    |
|                                 | DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load) |                               | 3.0 | 3.6             |      |
| V <sub>I</sub>                  | DC Input voltage range  |                               | 0   | V <sub>CC</sub> | V    |
| V <sub>O</sub>                  | DC output voltage range   |                               | 0   | V <sub>CC</sub> | V    |
| T <sub>amb</sub>                | Operating free-air temperature range  |                               | -40 | +85             | °C   |
| t <sub>r</sub> , t <sub>f</sub> | Input rise and fall times   | V <sub>CC</sub> = 2.3 to 3.0V | 0   | 20              | ns/V |
|                                 |   | V <sub>CC</sub> = 3.0 to 3.6V | 0   | 10              |      |

## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)  
 Voltages are referenced to GND (ground = 0V)

| SYMBOL                             | PARAMETER  | CONDITIONS   | RATING                        | UNIT |
|------------------------------------|--|--|-------------------------------|------|
| V <sub>CC</sub>                    | DC supply voltage  |  | -0.5 to +4.6                  | V    |
| I <sub>IK</sub>                    | DC input diode current   | V <sub>I</sub> < 0   | -50                           | mA   |
| V <sub>I</sub>                     | DC input voltage   | Note 1   | -0.5 to +4.6                  | V    |
| I <sub>OK</sub>                    | DC output diode current  | V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0                           | ± 50                          | mA   |
| V <sub>O</sub>                     | DC output voltage  | Note 1   | -0.5 to V <sub>CC</sub> + 0.5 | V    |
| I <sub>O</sub>                     | DC output source or sink current                                     | V <sub>O</sub> = 0 to V <sub>CC</sub>  | ± 50                          | mA   |
| I <sub>GND</sub> , I <sub>CC</sub> | DC V <sub>CC</sub> or GND current                                    |  | ± 100                         | mA   |
| T <sub>stg</sub>                   | Storage temperature range  |  | -65 to +150                   | °C   |
| P <sub>TOT</sub>                   | Power dissipation per package<br>-plastic thin-medium-shrink (TSSOP) | For temperature range: -40 to +125 °C<br>above +55°C derate linearly with 8 mW/K | 600                           | mW   |

### NOTE:

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

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## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

| SYMBOL            | PARAMETER                           | TEST CONDITIONS   | LIMITS                |                        |      | UNIT |
|-------------------|-------------------------------------|---|-----------------------|------------------------|------|------|
|                   |                                     |   | Temp = -40°C to +85°C |                        |      |      |
|                   |                                     |   | MIN                   | TYP <sup>1</sup>       | MAX  |      |
| V <sub>IH</sub>   | HIGH level Input voltage            | V <sub>CC</sub> = 2.3 to 2.7V   | 1.7                   | 1.2                    |      | V    |
|                   |                                     | V <sub>CC</sub> = 2.7 to 3.6V   | 2.0                   | 1.5                    |      |      |
| V <sub>IL</sub>   | LOW level Input voltage             | V <sub>CC</sub> = 2.3 to 2.7V   |                       | 1.2                    | 0.7  | V    |
|                   |                                     | V <sub>CC</sub> = 2.7 to 3.6V   |                       | 1.5                    | 0.8  |      |
| V <sub>OH</sub>   | HIGH level output voltage           | V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA                    | V <sub>CC</sub> - 0.2 | V <sub>CC</sub>        |      | V    |
|                   |                                     | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -4mA                             | V <sub>CC</sub> - 0.4 | V <sub>CC</sub> - 0.11 |      |      |
|                   |                                     | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -6mA                             | V <sub>CC</sub> - 0.6 | V <sub>CC</sub> - 0.17 |      |      |
|                   |                                     | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -4mA                             | V <sub>CC</sub> - 0.5 | V <sub>CC</sub> - 0.09 |      |      |
|                   |                                     | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -8mA                             | V <sub>CC</sub> - 0.7 | V <sub>CC</sub> - 0.19 |      |      |
|                   |                                     | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -6mA                             | V <sub>CC</sub> - 0.6 | V <sub>CC</sub> - 0.13 |      |      |
|                   |                                     | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA                            | V <sub>CC</sub> - 1.0 | V <sub>CC</sub> - 0.27 |      |      |
| V <sub>OL</sub>   | LOW level output voltage            | V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA                     |                       | GND                    | 0.20 | V    |
|                   |                                     | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4mA                              |                       | 0.07                   | 0.40 |      |
|                   |                                     | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA                              |                       | 0.11                   | 0.55 |      |
|                   |                                     | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4mA                              |                       | 0.06                   | 0.40 |      |
|                   |                                     | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 8mA                              |                       | 0.13                   | 0.60 |      |
|                   |                                     | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA                              |                       | 0.09                   | 0.55 |      |
|                   |                                     | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA                             |                       | 0.19                   | 0.80 |      |
| I <sub>I</sub>    | Input leakage current               | V <sub>CC</sub> = 2.3 to 3.6V;<br>V <sub>I</sub> = V <sub>CC</sub> or GND   |                       | 0.1                    | 5    | μA   |
| I <sub>OZ</sub>   | 3-State output OFF-state current    | V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>V <sub>O</sub> = V <sub>CC</sub> or GND |                       | 0.1                    | 10   | μA   |
| I <sub>CC</sub>   | Quiescent supply current            | V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0                                      |                       | 0.2                    | 40   | μA   |
| ΔI <sub>CC</sub>  | Additional quiescent supply current | V <sub>CC</sub> = 2.3V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0                                     |                       | 150                    | 750  | μA   |
| I <sub>BHL</sub>  | Bus hold LOW sustaining current     | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 0.7V <sup>2</sup>  | 45                    | -                      |      | μA   |
| I <sub>BHH</sub>  | Bus hold HIGH sustaining current    | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 1.7V <sup>2</sup>  | -45                   |                        |      | μA   |
|                   |                                     | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V <sup>2</sup>  | -75                   | -175                   |      |      |
| I <sub>BHLO</sub> | Bus hold LOW overdrive current      | V <sub>CC</sub> = 3.6V <sup>2</sup>   | 500                   |                        |      | μA   |
| I <sub>BHHO</sub> | Bus hold HIGH overdrive current     | V <sub>CC</sub> = 3.6V <sup>2</sup>   | -500                  |                        |      | μA   |

### NOTES:

1. All typical values are at T<sub>amb</sub> = 25°C.
2. Valid for data inputs of bus hold parts.

## 20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

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### AC CHARACTERISTICS FOR $V_{CC} = 2.5V \pm 0.2V$

GND = 0V;  $t_r = t_f \leq 2.0ns$ ;  $C_L = 30pF$ 

| SYMBOL            | PARAMETER   | WAVEFORM | LIMITS                  |                  |     | UNIT |
|-------------------|---|----------|-------------------------|------------------|-----|------|
|                   |   |          | $V_{CC} = 2.5 \pm 0.2V$ |                  |     |      |
|                   |   |          | MIN                     | TYP <sup>1</sup> | MAX |      |
| $t_{PHL}/t_{PLH}$ | Propagation delay<br>nAn to nYn                           | 1, 3     | 1.0                     | 2.9              | 4.6 | ns   |
| $t_{PZH}/t_{PZL}$ | 3-State output enable time<br>n $\overline{O}E$ n to nYn  | 2, 3     | 1.4                     | 3.9              | 6.4 | ns   |
| $t_{PHZ}/t_{PLZ}$ | 3-State output disable time<br>n $\overline{O}E$ n to nYn | 2,3      | 1.7                     | 2.2              | 5.9 | ns   |

**NOTE:**1. All typical values are at  $V_{CC} = 2.5V$  and  $T_{amb} = 25^\circ C$ .

### AC CHARACTERISTICS FOR $V_{CC} = 3.0V \pm 0.3V$

GND = 0V;  $t_r = t_f \leq 2.5ns$ ;  $C_L = 50pF$ 

| SYMBOL            | PARAMETER   | WAVEFORM | LIMITS                  |                     |     | LIMITS           |     | UNIT |
|-------------------|---|----------|-------------------------|---------------------|-----|------------------|-----|------|
|                   |   |          | $V_{CC} = 3.3 \pm 0.3V$ |                     |     | $V_{CC} = 2.7V$  |     |      |
|                   |   |          | MIN                     | TYP <sup>1, 2</sup> | MAX | TYP <sup>1</sup> | MAX |      |
| $t_{PHL}/t_{PLH}$ | Propagation delay<br>nAn to nYn                           | 1, 3     | 1.5                     | 2.9                 | 4.2 | 3.1              | 4.7 | ns   |
| $t_{PZH}/t_{PZL}$ | 3-State output enable time<br>n $\overline{O}E$ n to nYn  | 2, 3     | 1.6                     | 3.7                 | 5.4 | 4.4              | 6.5 | ns   |
| $t_{PHZ}/t_{PLZ}$ | 3-State output disable time<br>n $\overline{O}E$ n to nYn | 2, 3     | 1.8                     | 3.0                 | 4.7 | 3.2              | 5.2 | ns   |

**NOTES:**1. All typical values are at  $V_{CC} T_{amb} = 25^\circ C$ .2. Typical value is measured at  $V_{CC} = 3.3V$ .

# 20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

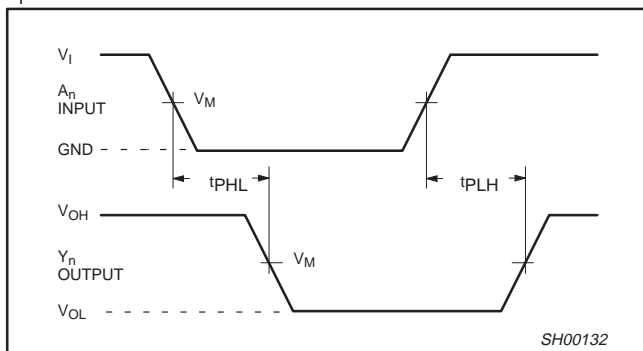
74ALVCH162827

## AC WAVEFORMS FOR $V_{CC} = 2.3V$ TO $2.7V$

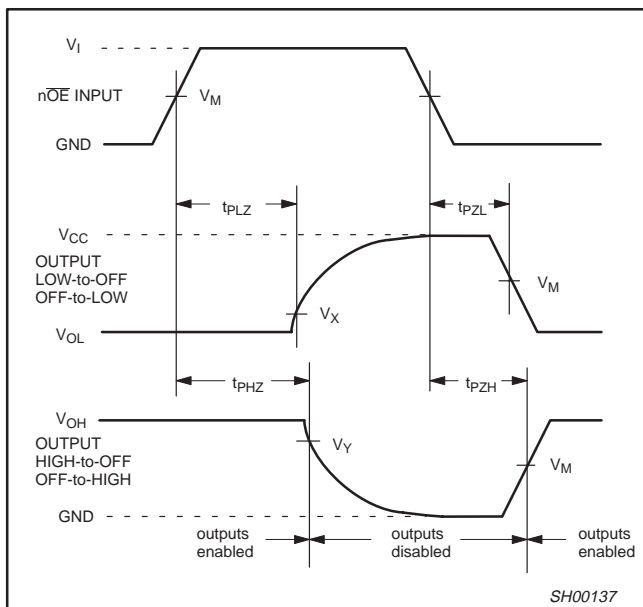
$V_M = 0.5 V_{CC}$   
 $V_X = V_{OL} + 0.15V$   
 $V_Y = V_{OH} - 0.15V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_I = V_{CC}$

## AC WAVEFORMS FOR $V_{CC} = 3.0V$ TO $3.6V$ AND $V_{CC} = 2.7V$ RANGE

$V_M = 1.5 V$   
 $V_X = V_{OL} + 0.3V$   
 $V_Y = V_{OH} - 0.3V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_I = 2.7V$



Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

## TEST CIRCUIT AND WAVEFORM

**Test Circuit for switching times**

**DEFINITIONS**  
 $R_L$  = Load resistor  
 $C_L$  = Load capacitance includes jig and probe capacitance  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**SWITCH POSITION**

| TEST              | $S_1$        | $V_{CC}$ | $V_I$    |
|-------------------|--------------|----------|----------|
| $t_{PLH}/t_{PHL}$ | Open         | < 2.7V   | $V_{CC}$ |
| $t_{PLZ}/t_{PZL}$ | $2 * V_{CC}$ | 2.7-3.6V | 2.7V     |
| $t_{PHZ}/t_{PZH}$ | GND          |          |          |

SV00906

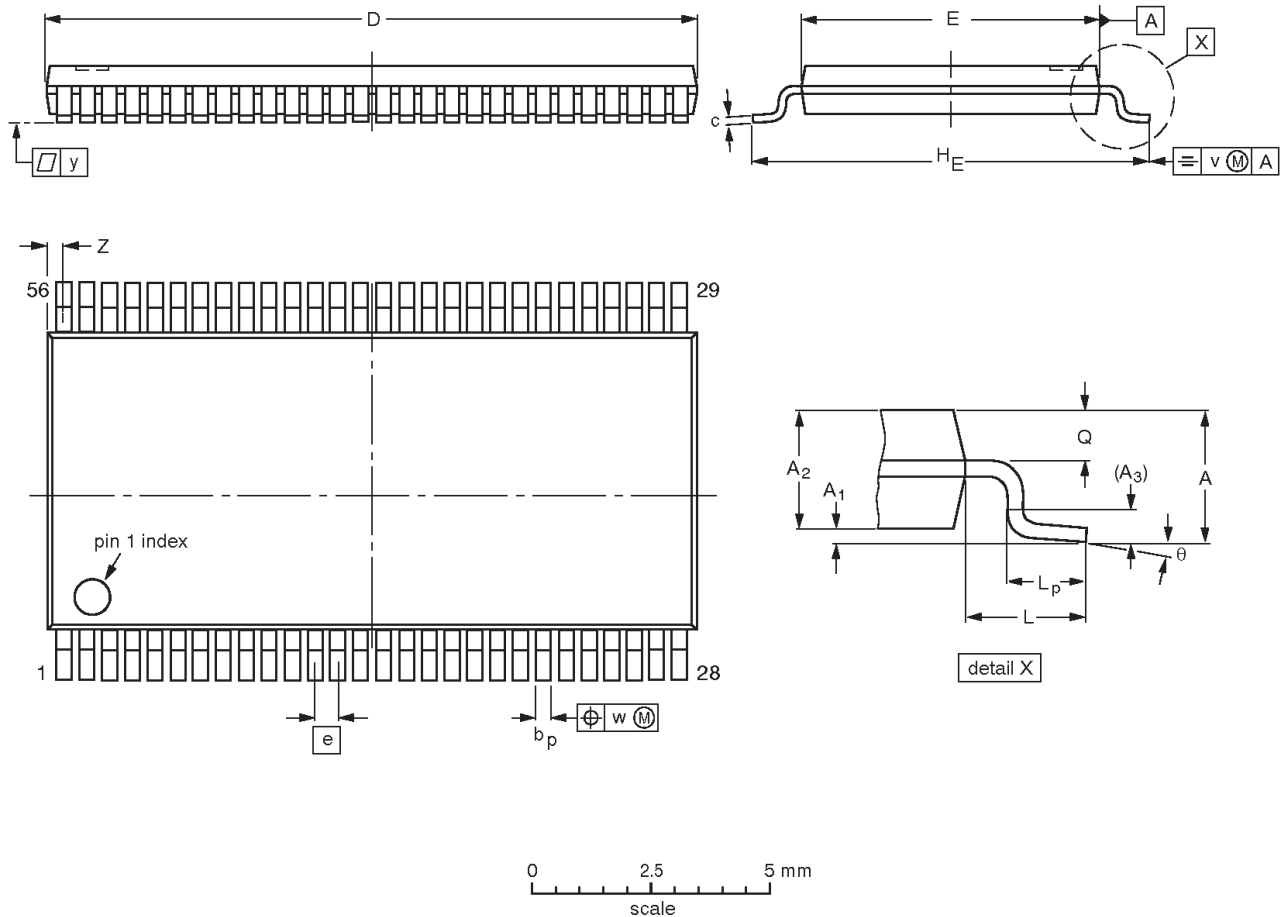
Waveform 3. Load circuitry for switching times

20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c          | D <sup>(1)</sup> | E <sup>(2)</sup> | e   | H <sub>E</sub> | L   | L <sub>p</sub> | Q            | v    | w    | y   | Z          | θ        |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|-----|----------------|-----|----------------|--------------|------|------|-----|------------|----------|
| mm   | 1.2    | 0.15<br>0.05   | 1.05<br>0.85   | 0.25           | 0.28<br>0.17   | 0.2<br>0.1 | 14.1<br>13.9     | 6.2<br>6.0       | 0.5 | 8.3<br>7.9     | 1.0 | 0.8<br>0.4     | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.5<br>0.1 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT364-1        |            | MO-153EE |      |  |                     | 93-02-03<br>95-02-10 |



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termination resistors (3-State)

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**NOTES**

# 20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

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## DEFINITIONS

| Data Sheet Identification        | Product Status                | Definition   |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i>   | <b>Formative or in Design</b> | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.   |
| <i>Preliminary Specification</i> | <b>Preproduction Product</b>  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| <i>Product Specification</i>     | <b>Full Production</b>        | This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.  |

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**811 East Arques Avenue**  
**P.O. Box 3409**  
**Sunnyvale, California 94088-3409**  
**Telephone 800-234-7381**

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